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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,373	06/19/2001	Eiji Hasegawa	NEC01P075-AMb	1068

466            7590            11/20/2002

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EXAMINER

BEREZNY, NEAL

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.	Applicant(s)
09/883,373	HASEGAWA, EIJI
Examiner	Art Unit
Neal Berezny	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

1) Responsive to communication(s) filed on 05 September 2002.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

4) Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-9 is/are rejected.

7) Claim(s) 2,5 and 8 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 19 June 2001 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

1) Notice of References Cited (PTO-892)      4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_ .

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)      5) Notice of Informal Patent Application (PTO-152)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 and 5 .      6) Other: \_\_\_\_\_ .

## **DETAILED ACTION**

1. Examiner acknowledges applicant's election, without traverse, of the Group I invention, claims 1-9, drawn to a method of making a semiconductor device.

### ***Drawings***

2. Figures 1a-1e, and 2a-2c should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

3. Claims 2, 5, and 8 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. These claims contain the limitation that the thickness of the gate insulating film be at least 0.2 nm. Since a single atomic layer of any of these dielectrics are over 0.2 nm, it is inherent that any layer formed with these dielectrics must be greater than 0.2 nm. Therefore, the claims are inherent and do not further limit the parent claims.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(a) as being anticipated by AAPA (Applicant's Admitted Prior Art). AAPA teaches a method of forming a plurality of gate insulating films, Fig.1a, comprising the steps of: injecting fluorine in other than the thinnest regions, fig.1b, el.103, oxidizing the plurality of regions, fig.1d, el.105, and then nitriding the surface of the oxide, page 10, line 10. Since a single atomic layer of any of these dielectrics are over 0.2 nm, it is inherent that any layer formed with these dielectrics must be greater than 0.2 nm.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as applied to claims 1 and 2 above, and further in view of Rodder et al.(6,251,761). AAPA does not teach the use of a remote nitrogen plasma for nitriding the gate oxide. Rodder teaches using remote plasma nitrogen for nitriding a gate oxide, col.3, ln.25-34. It

would have been obvious to one of ordinary skill in the art at the time of the invention to combine Rodder with AAPA to use a nitrogen plasma on the oxide to form a barrier layer from Boron contaminants and to prevent oxidation of the subsequent formation of the gate electrode, which would degrade the capacitance of the gate, col.3, ln.3-6.

8. Claims 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Rodder as applied to claims 1-3 above, and further in view of DeBusk et al.(6,140,187). Although Rodder does teach the formation of a gate stack, fig.2d and fig.1, el.104, the combination of AAPA and Rodder to not specifically state the specific well known steps involved in building a gate stack containing a gate insulator and a polysilicon gate electrode, nor the well known method of forming different gate thicknesses by forming gate stacks and then removing them from all but the desired regions, and then forming a new gate stack in the removed region with the second desired gate thickness. DeBusk teaches the steps for forming a gate stack, and the strategy of forming the well known method of forming different gate thicknesses by forming gate stacks and then removing them from all but the desired regions, and then forming a new gate stack in the removed region with the second desired gate thickness, fig.1, el.160 and 140, fig.2, el.260 and 270, col.4, ln.27-41. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Debusk with AAPA and Rodder to employ these well known methods of forming a gate stack to obtain gate insulators with different thicknesses, so that devices of different types could be manufactured on the same substrate with the same process, thereby reducing costs.

## CONCLUSION

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on Monday to Friday from 9:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached at (703) 306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Neal Berezny  
Patent Examiner

Art Unit 2823

11/18/02

  
Olik Chaudhuri  
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